REMARKS

Claims 1-20 are pending in the present application. Claims 1, 11, and 18 are amended herein. Claims 5, 12, and 19 have been canceled and their features have been incorporated into their respective independent claims. No new matter has been added.

The Examiner rejected claims 1-20 under 35 U.S.C § 103(a) as being obvious over U.S. Patent No. 5,025,407 ("Gulley") in view of U.S. Patent 5,061,866 ("El-Naggar"). Applicants have amended claims 1, 11, and 18 to include the features of dependant claims 5, 12, and 19 respectively. Applicants respectfully submit that independent claims 1, 11, and 18 and all claims depending therefrom, including claims 2-4, 6-10, 13-17, and 20, are patentable over the art of record for the following reasons.

The art of record fails to teach or suggest changing the sign of one or more selected vector components when the first signal indicates generation of the cross product component. Claim 1 as amended recites:

> a dual mode controller receiving the first and second vectors, the dual mode controller being configured to select vector components for evaluating a cross product component or a dot product in response to a first signal, the first signal indicting whether to generate a cross product component or a dot product, **wherein the dual mode controller changes the sign of one or more selected vector components when the first signal indicates generation of the cross product component**; and
>
> a dual mode unit coupled to receive the selected vector components for generating the gross product component or the dot product in response to the first signal and comprising a plurality of shared logic units that are used to generate the cross product component and the dot product (emphasis added).

El-Naggar teaches a vector scalar analog multiplier circuit and neural networks utilizing the circuit (El-Naggar, col. 2, ll. 60-63). The multiplier circuit provides an output voltage which is a linear function of the product of the amplitudes of at least one pair of input multiplicand voltages (Id., col. 2, ll. 63-66). A neuron circuit is created by connecting the output of the multiplier circuit to a circuit means that provides an output which is a sigmoidal function of its input and has its input connected to the output of an operational amplifier (Id., col. 3, ll. 60-65).

Gulley teaches a graphics coprocessor that receives an instruction statement from a main processor, determines the steps that must be taken to carry out the instruction statement

using its own microcode, performs the steps, and returns the results to the main processor (Gulley, col. 3, ll. 28-34). The coprocessor includes special registers that are available to the main processor, allowing the processor to retrieve the generated data when it needs to at its own clock rate (Id., col. 3, ll. 53-56).

The newly added features of claim 1, namely, the dual mode controller changes the sign of one or more selected vector components when the first signal indicates generation of the cross product component, were originally presented in now canceled claim 5. The Examiner rejected claim 5 as being "obvious because the computer instructions need proper operations to perform multiplier/adder for sufficiently generate the cross product vector's components." (Office Action at page 4).

However, the Examiner points to no reference in the prior art disclosing a dual mode controller changing the sign of one or more selected vector components when the first signal indicates generation of the cross product component. While the Examiner may be correct in asserting that it is necessary to change the sign of one or more of the selected vector components, that does not make it obvious to change the sign by the dual mode controller in response to the first signal. The cited prior art is insufficient to render the claimed invention obvious. If the Examiner maintains the rejection, the Applicant requests by direct reference to the prior art where this feature is disclosed or suggested.

Independent claims 11 and 18 have been amended to recite similar limitations as claim 1. It is therefore requested that independent claims 11 and 18 are therefore allowable for the same reasons as given for claim 1.

Claims 2-4, 6-10, 13-17, and 20 are all variously dependant on independent claims 1, 11, and 18. They are therefore allowable for at least the reasons given for the independent claims.

For all the foregoing reasons, Applicant respectfully submit that the pending claims patentably define over the cited art. Accordingly, a Notice of Allowance is respectfully requested. In the event, however, that the Examiner believes that the application is not allowable for any reason, the Examiner is encouraged to contact the undersigned attorney to discuss resolution of any remaining issues.

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